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EXAMINER	
STARK, JARRETT J	

ART UNIT	PAPER NUMBER
2823	

DATE MAILED: 03/31/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/827,534	ISHIKAWA, AKIRA	
	Examiner	Art Unit	
	Jarrett J. Stark	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 March 2006*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36,49-54 and 57-76* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36,49-54 and 57-76* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's\Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments filed 3/20/2006 have been fully considered but they are not persuasive.

Referring to applicant's arguments of the use of a photoresist mask to etch a part of a conductive layer. Edwards discloses the use of the photoresist mask to etch a conduductive layer forming a pattern. This technique is a VERY standard technique and notoriously well known to one of ordinary skill. Please refer to the previous response to arguments in the previous office action dated 12/20/2005, which lists numerous patents that disclose the use of a photoresist mask to etch a conductive layer. All arguments considering the novelty of the use of a photoresist mask to etch are considered moot.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-36, 49-54, and 57-76 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhang (US 5,814,529), in view of Edwards (US 3,189,973).

FIG. 5A

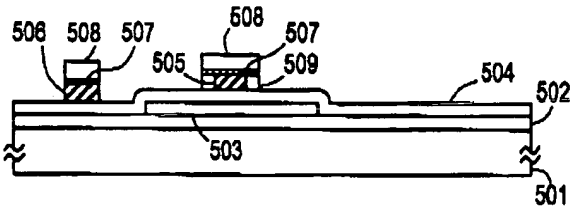


FIG. 5B

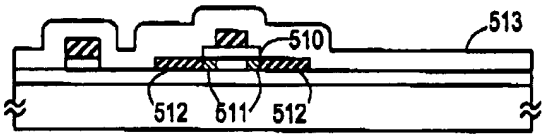


FIG. 5C

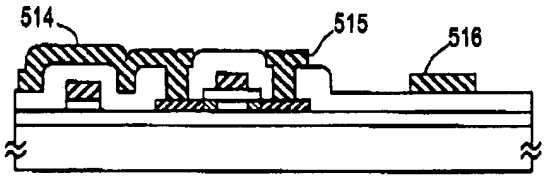


FIG. 5D

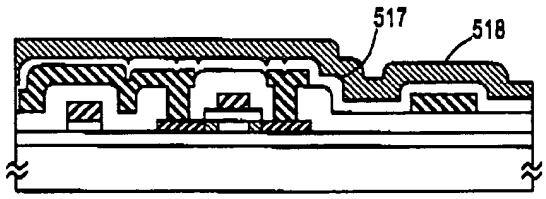


FIG. 5E

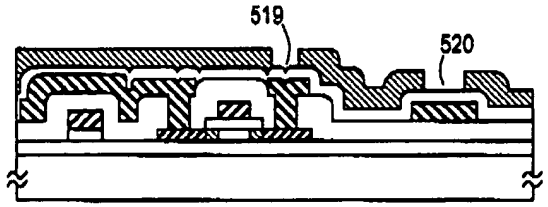
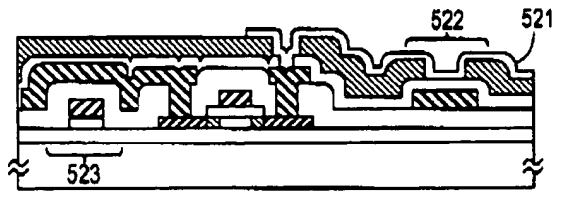


FIG. 5F



Regarding claims 1 & 49, Zhan teaches a method for manufacturing a semiconductor element comprising: forming a gate insulating film (Zhang, Fig 5A, [504]) over a semiconductor region;

forming a gate electrode (Zhang, Fig 5A, [505]) over the semiconductor region (Zhang, Fig 5A, [503]) with the gate insulating film interposed there between;

forming an insulating film covering the gate electrode; (Zhang, Fig 5A, [513])

exposing a part of the semiconductor region; (Zhang, Fig 5B →C)

forming a conductive film over the semiconductor region after exposing a part of the semiconductor region; ***The figure progression shows that potions of layer 513 is etched away to expose the "semiconductor region" 503 then a conductive film is deposited making contact with the semiconductor region.***

Zhang does not explicitly teach the method of forming a resist over the conductive film; (Zhang, Fig 5B →C)

removing a portion of the resist by etching the entire surface of the resist to form a resist mask;

etching a part of the conductive film by using the resist mask; and

etching a part of the etched conductive film.

Zhang discloses that the conductive film is "etched" but does not specifically say a "resist mask".

Edwards teahes the method of using a photoresist shape conductive films into a desired pattern. *(Edwards, col. 4, lines 1-3)*

This method is well-known and common knowledge in the art and is capable of instant and unquestionable demonstration as being well known. The use of resist masks has been a standard for at least the last two decades. Therefore it would be obvious to one of ordinary skill in the art at the time of the invention to form a resist mask and etch the conductive film.

By chemical etching the unmasked portion of the metal layer and the underlying oxide layer are removed to expose a part of the single crystal substrate. (Edwards, col. 4, lines 1-3)

Regarding wherein each source electrode and drain electrode is in contact with a side surface and an upper surface of the semiconductor region, Zhang, Fig 1E shows the electrodes 118 & 116 in contact with a upper and side "semiconductor region".

Regarding claims 2 & 50, Zhan teaches a method for manufacturing a semiconductor element comprising: forming a gate insulating film (Zhang, Fig 5A, [504]) over a semiconductor region;

forming a gate electrode (Zhang, Fig 5A, [505]) over the semiconductor region (Zhang, Fig 5A, [503]) with the gate insulating film interposed there between;

forming an insulating film covering the gate electrode; (Zhang, Fig 5A, [513])

exposing a part of the semiconductor region; (Zhang, Fig 5B →C)

forming a conductive film over the semiconductor region after exposing a part of the semiconductor region; ***The figure progression shows that potions of layer 513 is etched away to expose the "semiconductor region" 503 then a conductive film is deposited making contact with the semiconductor region.***

forming a resist over the conductive film;

removing a portion of the resist by etching the entire surface of the resist to form a resist mask;

etching a part of the conductive film by using the resist mask; and

etching a part of the etched conductive film and a part of the semiconductor region. (Edwards, col. 3-4, lines 74-3)

Regarding claims 3 & 51, Zhan teaches a method for manufacturing a semiconductor element comprising: forming a gate insulating film (Zhang, Fig 5A, [504]) over a semiconductor region;

forming a gate electrode over the semiconductor region (Zhang, Fig 5A, [503]) with the gate insulating film interposed there between;

exposing a part of the semiconductor region; (Zhang, Fig 5B →C)

forming a conductive film over the semiconductor region after exposing a part of *the semiconductor region;* ***The figure progression shows that potions of layer 513 is etched away to expose the "semiconductor region" 503 then a conductive film is deposited making contact with the semiconductor region.***

etching a part of the conductive film;

forming a resist over the conductive film;

removing a portion of the resist by etching the entire surface of the resist to form a resist mask; and

etching a part of the conductive film by using the resist mask. (Edwards, col. 3-4, lines 74-3)

Regarding claims 4 & 52, Zhan teaches a method for manufacturing a semiconductor element comprising: forming a gate insulating film (Zhang, Fig 5A, [504]) over a semiconductor region (Zhang, Fig 5A, [503]);

forming a gate electrode over the semiconductor region with the gate insulating film interposed there between; (Zhang, Fig 5A)

exposing a part of the semiconductor region; C

forming a conductive film over the semiconductor region after exposing a part of the semiconductor region; ***The figure progression shows that potions of layer 513 is etched away to expose the "semiconductor region" 503 then a conductive film is deposited making contact with the semiconductor region.***

etching a part of the conductive film and a part of the semiconductor region;

forming a resist over the conductive film;

removing a portion of the resist by etching the entire surface of the resist to form a resist mask; and

etching a part of the conductive film by using the resist mask. ((Edwards, col. 3-4, lines 74-3)

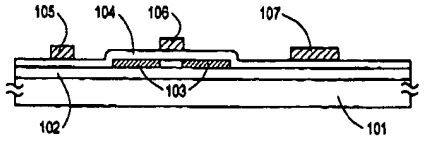
FIG. 1A 

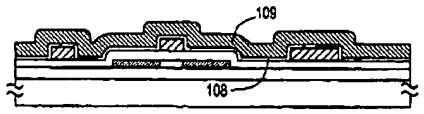
FIG. 1B 

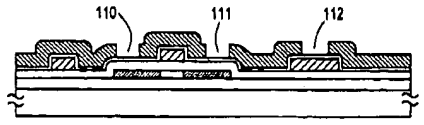
FIG. 1C 

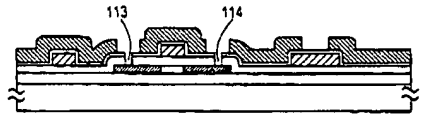
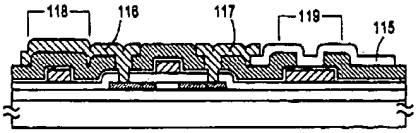
FIG. 1D 

FIG. 1E 

Regarding claims 5 & 53, Zhan teaches a method for manufacturing a semiconductor element comprising: forming a first insulating film over a semiconductor region;

forming a first conductive film over the first insulating film;

forming a second insulating film over the first conductive film;

forming a hard mask by etching the second insulating film;

etching the first conductive film by using the hard mask as a mask to form a gate electrode; (Zhang, Col. 3, lines 8-34)

From Zhang, Fig. 1A, it is obvious that the gate electrode 106 had to be formed by a mask. The use of a hard mask as claimed, for forming a gate electrode is common practice in the art which is briefly described by Zhang, Col. 3, lines 8-34.

forming a third insulating film over the semiconductor region;

etching the third insulating film to form a sidewall; (Zhang, Fig 1B, [108 or 109])

etching the first insulating film by using the sidewall and the hard mask as a mask to form a gate insulating film; (Zhang, Fig 1C-D, [110 & 113])

exposing a part of the semiconductor region; (Zhang, Fig 1D, [113])

forming a second conductive film; (Zhang, Fig 1D, [116])

forming a resist over the second conductive film;

removing a portion of the resist by etching the entire surface of the resist to form a resist mask;

etching a part of the second conductive film by using the resist mask as a mask; and (Edwards, col. 4, lines 1-3)

etching a part of the etched second conductive film and a part of the semiconductor region to form a source and drain electrode. (Zhang, Fig 1C-D, [116 & 117])

Regarding claims 6,54, Zhan teaches a method for manufacturing a semiconductor element comprising:

forming a first insulating film over a semiconductor region; (Zhang, Fig 1A, [104])

forming a first conductive film over the first insulating film; (Zhang, Fig 1A, [106])

forming a second insulating film over the first conductive film;

forming a hard mask by etching the second insulating film;

etching the first conductive film by using the hard mask as a mask to form a gate electrode;

From Zhang, Fig. 1A, it is obvious that the gate electrode 106 had to be formed by a mask. The use of a hard mask as claimed, for forming a gate electrode is common practice in the art which is briefly described by Zhang, Col. 3, lines 8-34.

forming a third insulating film over the semiconductor region; (Zhang, Fig 1B, [108 or 109])

etching the third insulating film to form a sidewall; (Zhang, Fig 1C-D, [110 & 113])

etching the first insulating film by using the sidewall and the hard mask as a mask to form a gate insulating film; (Zhang, Fig 1C-D, [108 & 1109])

exposing a part of the semiconductor region;

forming a second conductive film;

etching a part of the second conductive film;

forming a resist over the second conductive film;

removing a portion of the resist by etching the entire surface of the resist to form a resist mask; and (Edwards, col. 3-4, lines 74-3)

etching a part of the second conductive film by using the resist mask as a mask to form a source and drain electrode. (Zhang, Fig 1B-E, [116 & 117])

Regarding claim 7, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 1, wherein the resist mask is formed by developing after exposing an entire face of the resist to light.. (Edwards, col. 3-4, lines 74-3)

Regarding claim 8, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 1, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a part of the conductive film. (Edwards, col. 3-4, lines 74-3)

Regarding claim 9, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 1, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film. (Zhang, Fig 1A, [103])

Regarding claim 10, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 9, wherein the semiconductor substrate is a single crystal silicon substrate or a compound

semiconductor substrate. Using single crystal Si substrates is very common. Edwards (Col. 4, line 3) uses a "single crystal substrate".

Regarding claim 11, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 9, wherein the semiconductor thin film is a crystalline silicon film. (Zhang, Fig 1A, [103])

Regarding claim 12, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 2, wherein the resist mask is formed by developing after exposing an *entire face of the* resist to light. (Edwards, col. 3-4, lines 74-3)

Regarding claim 13, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 2, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a part of the conductive film. (Edwards, col. 3-4, lines 74-3)

Regarding claim 14, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 2, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film. (Zhang, Fig 1A, [103])

Regarding claim 15, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 14, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate. (Edwards. Col. 3, line 3)

Regarding claim 16, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 14, wherein the semiconductor thin film is a crystalline silicon film. (Zhang, Fig 1A, [103])

Regarding claim 17, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 3, wherein the resist mask is formed by developing after exposing an entire face of the resist to light. (Edwards, col. 3-4, lines 74-3)

Regarding claim 18, Zhan in view of Edwards teaches the method for *manufacturing* a semiconductor element according to Claim 3, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a part of the conductive film. (Edwards, col. 3-4, lines 74-3)

Regarding claim 19, Zhan in view of Edwards teaches the *method for manufacturing* a semiconductor element according to Claim 3, wherein the

semiconductor region is a semiconductor substrate or a semiconductor thin film. (Zhang, Fig 1A, [103])

Regarding claim 20, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 19, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate. (Edwards. Col. 3, line 3)

Regarding claim 21, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 19, *wherein* the semiconductor thin film is a crystalline silicon film. (Zhang, Fig 1A, [103])

Regarding claim 22, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 4, wherein the resist mask is formed by developing after exposing an entire face of the resist to light. (Edwards, col. 3-4, lines 74-3)

Regarding claim 23, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 4, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a part of the conductive film. (Edwards, col. 3-4, lines 74-3)

Regarding claim 24, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 4, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film. (Zhang, Fig 1A, [103])

Regarding claim 25, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 24, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate. (Edwards. Col. 3, line 3)

Regarding claim 26, Zhan in view of Edwards teaches the method for manufacturing *a* semiconductor element according to Claim 24, wherein the semiconductor thin film is a crystalline silicon film. (Zhang, Fig 1A, [103])

Regarding claim 27, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 5, wherein the resist mask is formed by developing after exposing an entire face of the resist to light. (Edwards, col. 3-4, lines 74-3)

Regarding claim 28, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 5, wherein the resist mask

is formed by removing a portion of the resist over a channel forming region, and exposing a part of the second conductive film. (Edwards, col. 3-4, lines 74-3)

Regarding claim 29, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 5, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film. (Zhang, Fig 1A, [103])

Regarding claim 30, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 29, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate. (Edwards. Col. 3, line 3)

Regarding claim 31, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 29, wherein the semiconductor thin film is a crystalline silicon film. (Zhang, Fig 1A, [103])

Regarding claim 32, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 6, wherein the resist mask is formed by developing after exposing an entire face of the resist to light. (Edwards, col. 3-4, lines 74-3)

Regarding claim 33, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 6, wherein the resist mask is formed by removing a portion of the resist over a channel forming region, and exposing a part of the second conductive film. (Edwards, col. 3-4, lines 74-3)

Regarding claim 34, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 6, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film. (Zhang, Fig 1A, [103])

Regarding claim 35, Zhan in view of Edwards teaches the method for manufacturing a semiconductor element according to Claim 34, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate. (Edwards. Col. 3, line 3)

Regarding claim 36, Zhan in view of Edwards teaches the method *for* manufacturing *a* semiconductor element according to Claim 34, wherein the semiconductor thin film is a crystalline silicon film. (Zhang, Fig 1A, [103])

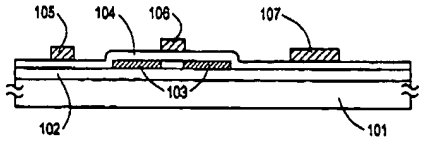
FIG. 1A 

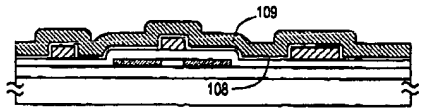
FIG. 1B 

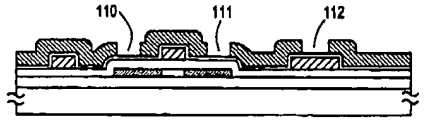
FIG. 1C 

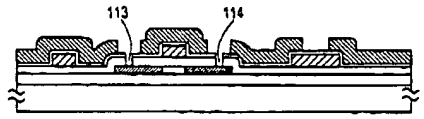
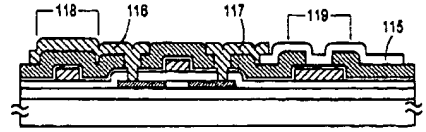
FIG. 1D 

FIG. 1E 

Regarding claims 57 & 63, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element comprising: forming a gate insulating film over a semiconductor region; (Zhang, Fig 1A)

forming a gate electrode over the semiconductor region with the gate insulating film interposed there between; (Zhang, Fig 1A)

forming an insulating film covering the gate electrode;

etching a portion of the insulating film to expose a part of the semiconductor region and to form portions of the insulating film remaining on at least side surfaces of the gate electrode; (Zhang, Fig 1A-E, [110 & 113])

forming a conductive film over the semiconductor region after exposing a part of the semiconductor region; (Zhang, Fig 1A-E, [116])

forming a resist over the conductive film;

removing a portion of the resist to form a resist mask;

etching a part of the conductive film by using the resist mask; and

etching a part of the etched conductive film, and (Edwards, col. 3-4, lines 74-3)

wherein said part of the semiconductor region is outside of the remaining portion of the insulating film. (Zhang, Fig 1A-E, [103])

Regarding claim 58, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 57, wherein the resist mask is formed by developing after exposing an entire face of the resist to light. (Edwards, col. 3-4, lines 74-3)

Regarding claim 59, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 57, wherein the resist mask is formed by etching an entire face of the resist, and exposing a part of the conductive film. (Edwards, col. 3-4, lines 74-3)

Regarding claim 60, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 57, wherein the

semiconductor region is a semiconductor substrate or a semiconductor thin film. (Zhang, Fig 1A-E, [103])

Regarding claim 61, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 60, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate. (Edwards. Col. 3, line 3)

Regarding claim 62, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 60, wherein the semiconductor thin film is a crystalline silicon film. (Zhang, Fig 1A-E, [103])

Regarding claims 64 & 69, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element comprising: forming a gate insulating film over a semiconductor region; (Zhang, Fig 1A)

forming a gate electrode over the semiconductor region with the gate insulating film interposed there between; (Zhang, Fig 1A)

forming an insulating film covering the gate electrode; (Zhang, Fig 1b, [109])

exposing parts of the semiconductor region; (Zhang, Fig 1A-E, [110 & 113])

forming a first conductive film over the semiconductor region after exposing the parts of the semiconductor region; (Zhang, Fig 1A-E, [116])

forming a resist over the first conductive film;

removing a portion of the resist to form a resist mask;

etching a part of the first conductive film by using the resist mask to form a second conductive film; and

etching a part of the second conductive film to form a source electrode and a drain electrode, (Edwards, col. 3-4, lines 74-3)

wherein each source electrode and drain electrode is in contact with a side surface and an upper surface of the semiconductor region. (Zhang, Fig 1E, [116 & 118])

Regarding claim 65, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 64, wherein the resist mask is formed by developing after exposing an entire face of the resist to light. (Edwards, col. 3-4, lines 74-3)

Regarding claim 66, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 64, wherein the resist mask is formed by etching an entire face of the resist, and exposing a part of the conductive film. (Edwards, col. 3-4, lines 74-3)

Regarding claim 67, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 64, wherein the semiconductor region is a semiconductor thin film. (Zhang, Fig 1A-E, [103])

Regarding claim 68, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 67, wherein the semiconductor thin film is a crystalline silicon film. (Zhang, Fig 1A-E, [103])

Regarding claims 70 & 76, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element comprising: forming a gate insulating film over a semiconductor region; (Zhang, Fig 1A, [104])

forming a gate electrode over the semiconductor region with the gate insulating film interposed tbere between; (Zhang, Fig 1A)

forming an insulating film covering the gate electrode; (Zhang, Fig 1B, [109])

exposing a part of the semiconductor region; (Zhang, Fig 1A-E, [110 & 113])

firming a first conductive film over the semiconductor region after exposing a part of the semiconductor region; (Zhang, Fig 1A-E, [116])

forming a resist over the first conductive film;

removing a portion of the resist to form a resist mask

etching a part of the first conductive film by using the resist mask to form a second conductive film; (Edwards, col. 3-4, lines 74-3)

etching a part of the second conductive film to form a source electrode and a drain electrode, (Zhang, Fig 1E, [116 & 118])

forming an interlayer insulating film over the source electrode and the drain electrode, and (Zhang, Fig 3C, [311])

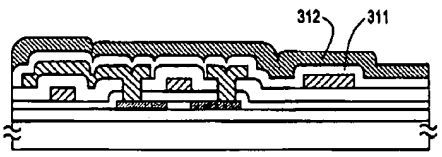
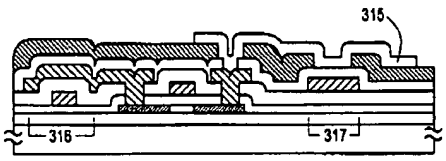
FIG. 3C 

FIG. 3E 

forming at least one connection wiring over the interlayer insulating film, (Zhang, Fig 3E, [315])

wherein said connection wiring is connected to one of the source electrode and the drain electrode through a hole of the interlayer insulating film.

wherein each source electrode and drain electrode is in contact with a side surface and an upper surface of the semiconductor region, Zhang, Fig 1E shows the electrodes 118 & 116 in contact with a upper and side "semiconductor region".

Regarding claim 71, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 70, wherein the resist mask is formed by developing after exposing an entire face of the resist to light. (Edwards, col. 3-4, lines 74-3)

Regarding claim 72, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 70, wherein the resist mask is formed by etching an entire face of the resist, and exposing a part of the conductive film. (Edwards, col. 3-4, lines 74-3)

Regarding claim 73, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 70, wherein the semiconductor region is a semiconductor substrate or a semiconductor thin film.

Regarding claim 74, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 73, wherein the semiconductor substrate is a single crystal silicon substrate or a compound semiconductor substrate. (Zhang, Fig 1A-E, [103])

Regarding claim 75, Zhan in view of Edwards teaches a method for manufacturing a semiconductor element according to Claim 73, wherein the semiconductor thin film is a crystalline silicon film. (Zhang, Fig 1A-E, [103])

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jarrett J. Stark whose telephone number is (571) 272-6005. The examiner can normally be reached on Monday - Thursday 7:00AM - 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JJS
March 24, 2006

W. DAVID COLEMAN
PRIMARY EXAMINER